Amod Holla

Electrical and Computer Engineering, Purdue University, West Lafayette
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Education

- **Ph.D. in Electrical and Computer Engineering**, Purdue University West Lafayette *May 2029*
  Advisor: Prof. Kaushik Roy **GPA: 4/4**
  Research: Advanced node memory design; mixed-signal circuit design for compute-in-memory; circuit design with emerging embedded memory technologies; hardware-algorithm co-design for efficient computing
- **B.Tech in Electrical Engineering**, Indian Institute of Technology Delhi *May 2024*
  Department Rank: 4/192, Best Bachelor Thesis in Electrical Engineering **GPA: 9.15/10**

Research Experience

- **Tapeout of a 22nm MRAM-Based Compute-in-Memory Accelerator** *August 2025 – May 2026*
  Collaboration with imec, Belgium
  - Part of a four-chip magnetoresistive RAM (MRAM) compute-in-memory prototype tapeout for accelerating DNN matrix–vector multiplications in GlobalFoundries (GF) 22nm.
  - Designed and laid out one of the four chips, including MRAM arrays, sensing peripherals, and calibration circuits for correcting analog non-idealities.
  - Built the shared tapeout infrastructure used across all four chips, including the GF 22nm RTL-to-GDSII flow for digital logic and a custom I/O pad ring.
- **Ternary Gain-cell Compute-in-Memory Macro in 22nm** *January 2026 – May 2026*
  - Developed a high-density gain-cell analog compute-in-memory macro with ternary bit-cell storage for highly quantized matrix-vector multiplications, reducing ADC conversion overhead for DNN acceleration.
  - Designed and laid out a 64×64 all-NMOS 3T gain-cell array with compute peripherals and self-calibration circuitry to mitigate transistor-mismatch-induced non-idealities.
  - Achieved 2.6× higher density than 8T-SRAM for equivalent compute-in-memory functionality.
- **In-Memory Probabilistic Computing for Combinatorial Optimization** *April 2025 – July 2025*
  Collaboration with imec, Belgium
  - Developed a compute-in-memory architecture for accelerating NP-hard large-scale routing problems.
  - Designed 8T-SRAM arrays and sense amplifiers integrating spin-based devices for probabilistic computing.
  - Developed control logic to execute in-memory optimization cycles for large-scale routing problems.
  - Cycle-accurate evaluations of the ASIC implementation project 7 and 14 orders-of-magnitude improvement in time-to-solution and energy efficiency, respectively, compared with a CPU, with $<$15% quality loss.

Current Research

- **In-Memory Boolean Operations in 2nm Nanosheet FET Technology** *August 2026 – Present*
  Collaboration with imec, Belgium
  - Developing 8T-SRAM arrays and supporting digital logic in imec 2nm nanosheet FET technology for in-memory Boolean operations, targeting accelerated k-nearest-neighbor search in graph-based combinatorial optimization.

Selected Publications

- **A. Holla**, S. Chatterjee, S. Sen, A. Mukherjee, F. García-Redondo, D. Biswas, F. Iacopi, and K. Roy, "LIMO: Low-power in-memory-annealer and matrix-multiplication primitive for edge computing," *npj Unconventional Computing*, 2026.
- **A. Holla**, M. Mukherjee, A. Mukherjee, and K. Roy, "ROSETTA: ROM-Overlaid STT-MRAM for Efficient MVM and Softmax Operations Towards Accelerating Transformer Inference," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2026.
- S. Yoo, **A. Holla**, S. Sanyal, D. E. Kim, F. Iacopi, D. Biswas, J. Myers, and K. Roy, "TAXI: Traveling Salesman Problem Accelerator with X-bar-based Ising Macros Powered by SOT-MRAMs and Hierarchical Clustering," *ACM/IEEE Design Automation Conference (DAC)*, 2025.
- R. S. Yadav, P. Gupta, **A. Holla**, K. I. A. Khan, P. K. Muduli, and D. Bhowmik, "Demonstration of Synaptic Behavior in a Heavy-Metal-Ferromagnetic-Metal-Oxide-Heterostructure-Based Spintronic Device for On-Chip Learning in Crossbar-Array-Based Neural Networks," *ACS Applied Electronic Materials*, 2023.

Technical Skills

EDA Tools: Cadence Virtuoso, Genus, Innovus **HDLs & Programming:** Verilog, SystemVerilog, Python, C
Circuit & VLSI Design: Custom circuit design and layout, synthesis, PNR, STA, RTL-to-GDSII flow, tapeout

Relevant Coursework

MOS VLSI Design, Advanced VLSI Design, Solid State Devices, AI Hardware, CMOS Analog IC Design